REMARKS/ARGUMENTS

Claims 1, 2, 6, and 7 are pending in this application. By this Amendment, Applicant AMENDS claims 1 and 2, and ADDS new claims 6 and 7.

Support for newly added claims 6 and 7 can be found, for example, in paragraphs [0021] and [0037] of Applicant's specification and in Figs. 1-6C of Applicant's drawings.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Mariko (JP 03-276730) in view of Hirano et al. (U.S. 6,849,908). Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishiyama et al. (U.S. 7,087,969) in view of Mariko.

Applicant respectfully traverses the prior art rejections of claims 1 and 2.

Claim 1 has been amended to recite:

> A semiconductor device, comprising:
> a well of a first conductive type formed in an upper layer of a substrate;
> a low-concentration layer of the first conductive type having a lower impurity concentration than the well, the low-concentration layer being formed in an extreme surface layer of a channel portion of the well;
> a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film, the high-k gate dielectric layer being formed on the low-concentration layer;
> a gate electrode formed on the high-k gate dielectric layer;
> **extension regions of a second conductive type formed in an upper layer of the well, the extension regions sandwiching the low-concentration layer**; and
> source/drain regions of the second conductive type formed in an upper layer of the well, the source/drain regions sandwiching the low-concentration layer and the extension regions; wherein
> **a depth of the low-concentration layer from an upper surface of the substrate is smaller than a depth of the extension regions from the upper surface of the substrate**. (emphasis added)

The Examiner alleged that Mariko teaches "a low-concentration layer 7 of the first conductive p-type having a lower impurity concentration than the well 8, the low-concentration layer 7 being formed in an extreme surface layer of a channel portion of the well 8." The Examiner acknowledged that Mariko fails to teach or suggest a gate dielectric layer being a high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film. The Examiner further alleged that Hirano et al. teaches a high-k gate dielectric layer. Thus, the

Examiner concluded that it would have been obvious to one having ordinary skill in the art at the time of the invention to "form a high-k gate dielectric layer/a metal silicate layer served as a gate dielectric film having a higher dielectric constant than a silicon oxide film, as taught by Hirano in the semiconductor device as disclosed by [Mariko] in order to suppress leakage current flowing through the gate dielectric film (see Hirano, col. 6, lines 24-26)." However, Applicant submits that the combination of Mariko and Hirano et al. fails to teach each and every one of the features recited in Applicant's claim 1.

Applicant has amended claim 1 to recite the features of "extension regions of a second conductive type formed in an upper layer of the well, the extension regions sandwiching the low-concentration layer" and "a depth of the low-concentration layer from an upper surface of the substrate is smaller than a depth of the extension regions from the upper surface of the substrate." Support for these feature is found, for example, in paragraphs [0021] and [0037] of Applicant's specification and in Figs. 1-6C of Applicant's drawings.

Neither Mariko nor Hirano et al. teaches or suggests these features.

Mariko teaches a MOS transistor that includes a high concentration p-type semiconductor region 8, a low concentration p-type surface layer 7, and a high concentration n-type diffusing layer 6, as shown in Fig. 1 of Mariko. However, Mariko does not teach or suggest high concentration n-type extension regions that are arranged to be higher than the low concentration p-type surface layer 7. Accordingly, Mariko does not teach or suggest the features of "extension regions of a second conductive type formed in an upper layer of the well, the extension regions sandwiching the low-concentration layer" and "a depth of the low-concentration layer from an upper surface of the substrate is smaller than a depth of the extension regions from the upper surface of the substrate" as is recited in Applicant's claim 1.

Hirano et al. merely teaches that a metal silicate layer 12a and a gate electrode 24 are formed on a main surface of a silicon substrate 10, as shown in Fig. 4 of Hirano et al. Accordingly, Hirano et al. also fails to teach or suggest the features of "extension regions of a second conductive type formed in an upper layer of the well, the extension regions sandwiching the low-concentration layer" and "a depth of the low-concentration layer from an upper

surface of the substrate is smaller than a depth of the extension regions from the upper surface of the substrate" as is recited in Applicant's claim 1.

Thus, Applicant respectfully submits that Mariko and Hirano et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of features recited in claim 1 of the present application.

Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Mariko in view of Hirano et al.

Claim 2 has been amended to recite:

A complementary semiconductor device having a n-type circuit region and a p-type circuit region, comprising:

a p-type well formed in an upper layer of a substrate of the n-type circuit region;

a n-type well formed in an upper layer of the substrate of the p-type circuit region;

a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, the p-type low-concentration layer having a lower impurity concentration than the p-type well;

a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well, the n-type low-concentration having a lower impurity concentration than the n-type well;

a high-k gate dielectric layer formed on the p-type and n-type low-concentration layers, the high-k gate dielectric layer having a higher dielectric constant than a silicon oxide film;

a gate electrode formed on the high-k gate dielectric layer;

n-type extension regions formed in an upper layer of the p-type well, the n-type extension regions sandwiching the p-type concentration layer;

n-type source/drain regions formed in an upper layer of the p-type well, the n-type source/drain regions sandwiching the p-type low-concentration layer and the n-type extension regions;

p-type extension regions formed in an upper of the n-type well, the p-type extension regions sandwiching the n-type low-concentration layer; and

p-type source/drain regions formed in an upper layer of the n-type well, the p-type source/drain regions sandwiching the n-type low-concentration layer and the p-type extension regions; wherein

a depth of the p-type low-concentration layer from an upper surface of the substrate is smaller than a depth of the n-type extension regions from the upper surface of the substrate; and

> **a depth of the n-type low-concentration layer from the upper surface of the substrate is smaller than a depth of the p-type extension regions from the upper surface of the substrate**. (emphasis added)

The Examiner alleged that "Nishiyama discloses in Fig. 1 and related texts as set forth in col. 4, line 45-col. 5, line 30, a complementary semiconductor device having a n-type circuit region 3 and a p-type circuit region 5." The Examiner acknowledged that Nishiyama fails to teach or suggest a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, and a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well. The Examiner further alleged that Mariko teaches "a low-concentration layer 7 of the first conductive p- type having a lower impurity concentration than the well 8, the low-concentration layer 7 being formed in an extreme surface layer of a channel portion of the well 8." Thus, the Examiner concluded that it would have been obvious to one having ordinary skill in the art at the time of the invention "to provide a low-concentration layer formed in an extreme surface layer of a channel portion of the well having a lower impurity concentration than the well ... in order to decrease a threshold voltage and to suppress a short-channel effect."

Applicant has amended claim 2 to recite the features of "n-type extension regions formed in an upper layer of the p-type well, the n-type extension regions sandwiching the p-type concentration layer," "p-type extension regions formed in an upper of the n-type well, the p-type extension regions sandwiching the n-type low-concentration layer," "a depth of the p-type low-concentration layer from an upper surface of the substrate is smaller than a depth of the n-type extension regions from the upper surface of the substrate," and "a depth of the n-type low-concentration layer from the upper surface of the substrate is smaller than a depth of the p-type extension regions from the upper surface of the substrate." Support for these feature is found, for example, in paragraphs [0021] and [0037] of Applicant's specification and in Figs. 1-6C of Applicant's drawings.

Neither Nishiyama et al. nor Mariko teaches or suggests these features.

The Examiner admitted that Nishiyama et al. "fails to teach or suggest a p-type low-concentration layer formed in an extreme surface layer of a channel portion of the p-type well, and a n-type low-concentration layer formed in an extreme surface layer of a channel portion of the n-type well." The Examiner relied on Mariko to teach these features. Accordingly, Nishiyama et al. fails to teach or suggest the features of "n-type extension regions formed in an upper layer of the p-type well, the n-type extension regions sandwiching the p-type concentration layer," "p-type extension regions formed in an upper of the n-type well, the p-type extension regions sandwiching the n-type low-concentration layer," "a depth of the p-type low-concentration layer from an upper surface of the substrate is smaller than a depth of the n-type extension regions from the upper surface of the substrate," and "a depth of the n-type low-concentration layer from the upper surface of the substrate is smaller than a depth of the p-type extension regions from the upper surface of the substrate," as recited in Applicant's claim 2.

However, as discussed above, Mariko teaches a MOS transistor that includes a high concentration p-type semiconductor region 8, a low concentration p-type surface layer 7, and a high concentration n-type diffusing layer 6, as shown in Fig. 1 of Mariko. However, Mariko does not teach or suggest high concentration n-type extension regions that are arranged to be higher than the low concentration p-type surface layer 7. Accordingly, Mariko does not teach or suggest the features of "n-type extension regions formed in an upper layer of the p-type well, the n-type extension regions sandwiching the p-type concentration layer," "p-type extension regions formed in an upper of the n-type well, the p-type extension regions sandwiching the n-type low-concentration layer," "a depth of the p-type low-concentration layer from an upper surface of the substrate is smaller than a depth of the n-type extension regions from the upper surface of the substrate," and "a depth of the n-type low-concentration layer from the upper surface of the substrate is smaller than a depth of the p-type extension regions from the upper surface of the substrate," as recited in Applicant's claim 2.

Accordingly, Applicant respectfully submits that Nishiyama et al. and Mariko, applied alone or in combination, fail to teach or suggest the unique combination and arrangement of

features recited in claim 2 of the present application.

Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Nishiyama et al. in view of Mariko.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1 and 2 are allowable. Claims 6 and 7 depend upon claims 1 and 2, and are therefore allowable for at least the reasons that claims 1 and 2 are allowable.

To the extent necessary, Applicant petitions the Commissioner for a ONE-month extension of time, extending to November 10, 2009, the period for response to the Office Action dated July 10, 2009.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Dated: November 6, 2009

/Erik Preston #64,733/
Attorneys for Applicant

KEATING & BENNETT, LLP
1800 Alexander Bell Drive, Suite 200
Reston, VA 20191
Telephone: (571) 313-7440
Facsimile: (571) 313-7421

Joseph R. Keating
Registration No. 37,368

Erik Preston
Registration No. 64,733